OBJECTIONS TO THE DRAWINGS

The drawings were objected to under 37 CFR § 1.83(a) on the ground that the drawings do not show a frequency acquisition loop that is configured to adjust a frequency between an extracted clock signal and a binary signal and a frequency of the extracted clock signal, as recited in pending claims 5, 6, 18, 19, 22, 23, 25, and 26. Applicant respectfully submits that the amendments to claims 5, 6, 18, 19, 22, 23, and 25 to recite a "reference signal" or "reference clock" instead of "binary signal," obviate this objection. Claim 26 has been canceled, rendering this objection moot. Therefore, Applicant respectfully requests that these objections be withdrawn.

OBJECTION TO THE SPECIFICATION

The Office Action issued an objection to the specification corresponding to the objection to the drawings on the ground that the detailed description does not describe a frequency acquisition loop that maintains a frequency between an extracted clock signal and a binary signal. Applicant respectfully submits that this objection has also been obviated by the amendments as described with reference to the objection to the drawings. Accordingly, Applicant respectfully requests that this objection be withdrawn.

CLAIM OBJECTIONS

Claims 5, 6, 18, 19, 22, 23, 25, and 26 were objected to on the ground that "binary signal" should be "reference signal." Applicant respectfully submits that the amendments to the claims overcome these objections. Accordingly, Applicant requests that these objections be withdrawn.

§ 112 REJECTIONS

Claims 7, 25, 26, and 28 were rejected under 35 U.S.C. § 112, first paragraph, on the ground that the specification does not enable one of ordinary skill in the art to make and/or use the invention. Applicant respectfully submits that the specification and figures do provide an enabling disclosure of the claims, as amended.

Claim 7 has been canceled, but claim 1 has been amended to recite that the multiplier is "configured to apply an equalization coefficient to the recovered equalized data to generate the equalized feedback signal," and that the clock and data recovery circuit "is configured to iterate the equalization coefficient until the clock and data recovery circuit synchronizes with a frequency of the equalized data."

Reference will first be made to the figures for an overview of these operations, and then to the specification. FIG. 4 shows the multiplier 480 coupled to the retimer 470. The multiplier 480 applies the equalization coefficient to the recovered equalized data to generate the equalized feedback signal 450. The clock and data recovery circuit 420 generates the extracted clock signal 430 from the equalized data (via the slicer 460).

FIG. 5 shows the clock and data recovery circuit 500, which receives the binary signal D3/50 as data 565. A frequency lock detector 510 receives an extracted clock signal 515(a) divided by a frequency divider 525. The extracted clock signal 515(a) is generated from the binary signal D3/50 or data 565 via, among other components, a phase detector 560, charge pump 570, and an oscillator 515. The frequency lock detector 510 measures a difference in frequency between the frequency divided extracted clock signal 525(a) and a reference clock 520, and activates a real time open loop optimization circuit 590 if the difference exceeds a threshold. The real time open loop optimization circuit 590 in turn controls the equalization coefficient of the multiplier 480.

Page 7, lines 24-30 of the specification discloses that "the equalization coefficient is automatically iterated until the clock and data recovery circuit 420 synchronizes with the frequency of the equalized data at which point a real time optimization loop (not shown) adjusts the equalization coefficient to reduce or minimize the inter-symbol interference in the equalized data." The clock and data recovery circuit 420 generates the extracted clock signal 430. Page 5,

line 35 to page 6, line 6. The binary signal D3 is converted from the output of the summer 430, which in turn receives input from the equalized feedback signal 450.

The real time open loop optimization circuit 590 generates the equalization coefficient of the multiplier 480. Page 7, line 31 to page 8, line 6; page 6, lines 21-24. The frequency lock detector 510, in turn, controls the real time open loop optimization circuit 590. Page 7, lines 33-35. The frequency lock detector 510 activates the real time open loop optimization circuit 590 based on a shift between the reference clock 520 and the divided signal 525(a). Page 9, lines 27-30; page 10, lines 11-15. The data 565 received by the clock and data recovery circuit 500 is the binary signal D3/50 generated by the decision feedback equalizer 410. Page 10, lines 19-23. The clock and data recovery circuit ensures that the data signal 565 and the output signal 515(b) have a desired phase relationship. Page 11, lines 19-22. Applicant respectfully submits that at least these portions of the disclosure enable amended claim 1.

Claim 25 has been amended to recite that "the retiming includes modifying the equalization coefficient to synchronize frequencies of the extracted clock signal and the reference clock." As shown in FIG. 5, the phase and frequency detector 505 receives as inputs the divided extracted clock signal 525(a) and the reference clock 520. The phase and frequency detector 505 thereby determines the frequency difference between the feedback signal 515(a) and the reference clock 520. Page 8, lines 16-19. The phase and frequency detector 505 generates an output signal based on the frequency difference, which modifies the extracted clock signal 515(a) (which in turn modifies the signal generated by the frequency lock detector 510, which controls the real time open loop optimization circuit 590, which controls the equalization coefficient, as described above), until the difference between the extracted clock frequency and reference clock frequency falls within a particular threshold. Page 8, line 28 to page 9, line 27. Applicant respectfully submits that at least these portions of the disclosure enable claim 25.

Claim 26 has been canceled, rendering this rejection moot. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

Claim 28 has been amended to recite, "the clock and data recovery circuit is configured to adjust the equalization coefficient based on a frequency difference exceeding a threshold, the frequency difference being based on a frequency of a reference clock included in the clock and data recovery circuit and a frequency of a divided signal, the divided signal being generated from

the extracted clock signal." Applicant respectfully submits that this claim is enabled for the reasons discussed above, and requests that this rejection be withdrawn.

Claims 8 and 20 were rejected on the ground that the specification does not describe the multiplier 480 as changing or adjusting the equalization coefficient. These claims have been canceled, rendering these rejections moot. Accordingly, Applicant respectfully requests that these rejections be withdrawn.

§ 103 REJECTIONS

The Office Action rejected claims 1-5, 17, 18, 21, 22, and 24 under 35 U.S.C. § 103(a) as being unpatentable over what the Office Action described as "admitted prior art" in view of Tomita, U.S. Patent No. 6,931,088. Applicant respectfully submits that the amendments to these claims overcome these rejections.

Claim 1 has been amended to recite that the decision feedback equalizer includes, "a multiplier coupled to the retimer, the multiplier being configured to apply an equalization coefficient to the recovered equalized data to generate the equalized feedback signal," and that "the clock and data recovery circuit is configured to iterate the equalization coefficient until the clock and data recovery circuit synchronizes with a frequency of the equalized data." Applicant respectfully submits that these recited portions of amended claim 1 are not disclosed or suggested by the "admitted prior art" or Tomita, which do not disclose changing an equalization coefficient based on a frequency, and requests that the rejection of claim 1 be withdrawn. Applicant further requests that the rejections of claims 2-5 be withdrawn due to their dependence on allowable claim 1.

Claim 17 has been amended to recite that the clock and data recovery circuit is configured to "vary the equalization coefficient based on a difference between a frequency of the extracted clock signal and a frequency of a reference clock." Applicant respectfully submits that this portion of amended claim 17 is not disclosed or suggested by the "admitted prior art" or Tomita, and requests that the rejection of claim 17 be withdrawn. Applicant further requests that the rejections of claims 18, 21, and 22 be withdrawn due to their dependence on allowable claim 17. Applicant requests that the rejection of claim 24 be withdrawn due to the cancellation of claim 24.

The Office Action rejected claims 5, 6, 18, 19, 22, and 23 as being unpatentable over the "admitted prior art" in view of Tomita and further in view of Kim et al., U.S. Patent No. 6,670,853. Applicant respectfully submits that the amendments to claims 1 and 17, upon which these claims depend, overcome these rejections because no combination of the "admitted prior art," Tomita, and/or Kim properly discloses or suggests the elements of these claims. Accordingly, Applicant respectfully requests that these rejections be withdrawn.

Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the "admitted prior art" in view of Tomita, Kim, and Lin et al., U.S. Patent Pub. No. 2004/0120422 A1. Claim 8 has been canceled, rendering this rejection moot. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

Claims 20 and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the references as applied to claims 19 and 1, and further in view of Welland et al., U.S. Patent No. 5,786,951. Claim 20 has been canceled, rendering this rejection moot, and Applicant respectfully requests that this rejection be withdrawn. Applicant further requests that the rejection of claim 27 be withdrawn due to its dependence on allowable claim 1, as Welland et al. does not compensate for the deficiencies of the references discussed above with respect to the rejection of claim 1.

NEWLY ADDED CLAIMS

Claims 29-32 have been added, with claim 29 being independent. Applicant respectfully submits that these claims are allowable at least because none of the cited references disclose or suggest "a clock and data recovery circuit configured to control the equalization coefficient based on a signal which combines the received data with the equalized feedback signal and a reference clock," as recited in claim 29, upon which claims 30-32 depend.

CONCLUSION

Applicant respectfully submits that claims 1-6, and 17-19, 21-23, 25, and 27-32 are in condition for allowance, and earnestly requests notification to that effect. The Examiner is invited to telephone Applicant's attorney (208-286-1013) to facilitate prosecution of this application.

No fees are believed to be due at this time. If necessary, please charge any additional fees or credit any overpayment to Deposit Account No. 50-3521, referencing Attorney Docket No. BU3368/0033-097001.

Respectfully submitted,

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208-286-1013

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